WHAT IS CLAIMED IS:

1. A method of manufacturing a trench field effect transistor on a substrate having a first conductivity type, the method comprising the steps of:

forming a first trench extending into the substrate;

lining the first trench with dielectric material;

substantially filling the first trench with conductive material to form a gate electrode of the field effect transistor;

forming a body region having a second conductivity type in the substrate;

forming a source region having the first conductivity type inside the body region and adjacent to the first trench;

forming a second trench adjacent to said source region and extending into the body region below the source region; and

filling the second trench with high conductivity material for making contact to the body region.

2. The method of claim 1 wherein the step of filling the second trench with high conductivity material for making contact to the body region also makes contact to the source region.

3. The method of claim 2 wherein the step of filling the second trench with high conductivity material comprises a self-aligned masking step for making contact with both the body region and the source region.

4. The method of claim 2 further comprising a step of implanting impurities of the second conductivity type into the body region under the second trench before the step of filling the second trench.

5. The method of claim 4 further comprising a step of heating the substrate after the step of implanting to drive the impurities further into the body region.

6. The method of claim 2 further comprising a step of forming a thin layer of barrier metal between the high conductivity material and the body region.

7. The method of claim 6 wherein the high conductivity material comprises aluminum and the thin layer of barrier metal comprises titanium.

8. The method of claim 2 wherein the step of forming the second trench comprises a step of etching silicon through the source and body regions.

9. The method of claim 2 wherein the second trench is shallower than the first trench.

10. The method of claim 2 wherein the second trench is approximately as deep as the first trench.

11. The method of claim 2 wherein the second trench is deeper than the first trench.

12. The method of claim 8 wherein the step of etching etches the silicon at an angle resulting in a slanted edge along the etched side of the source region.

Sub B2

13. A process for manufacturing a trench field effect transistor comprising the steps of:

etching a first trench in a substrate having a first conductivity type;

lining the first trench with a layer of dielectric material;

substantially filling the trench with polysilicon;

implanting impurities of a second conductivity type into the substrate to form a body region having the second conductivity type over the substrate;

implanting impurities of the first conductivity type inside the body region to form a source region adjacent to the first trench;

etching a second trench through the source region and into the body region; and

filling the second trench with metal making contact with both the source region and the body region.

14. The process of claim 13 further comprising a step of implanting impurities of the second conductivity type into the body region under the second trench before the step of filling the second trench with metal.

15. The process of claim 13 wherein the step of etching the second trench etches the second trench to a shallower depth than the first trench.

16. The process of claim 13 wherein the step of etching the second trench etches the second trench to substantially a same depth as the first trench.

17. The process of claim 13 wherein the step of etching the second trench etches the second trench deeper than the first trench.

add AC3